Remarks

Claims 1-11 remain in the application. A number of non-substantive editorial corrections have been made to the claims.

The Examiner objects to the drawings under 37 CFR 1.84(p)(5) for including reference characters not mentioned in the text.

Number "2" in FIG. 1 is, contrary to the Examiner position mentioned in page 7, line 12.

The text on pages 10 and 11 have been amended to include CE*, DATA, ROW/COL, and WE* of FIG. 3 although it is felt that the existing text was sufficient for the ordinary reader. It is noted that the filed text contains references to WE* and CE* in descriptions of circuitry more detailed than FIG. 3. The text on page 17 has been amended to include MICROPROCESSOR INTERFACE, DUTY FACTOR, ROW ADDR, COLUMN ADDR, AND WRITE ENABLE OF FIG. 7. The text on page 18 has been amended for MAJOR and MINOR of FIG. 9.

The objection to FIG. 12 is not understood. All the objected symbols CE*, CE1*, CE2*, CMP, R8P, and R8P* are described in the paragraph introducing FIG. 12 at page 20, lines 4-24.

The symbols objected to in FIG. 17 are described in more detail with reference to similar circuitry in FIG. 16 at page 24, line 3, 5, and 10. This passage has been amended to explicitly include RESET.

The Examiner objects to the drawings under 37 CFR 1.84(p)(4) because reference "240" has been used to designate both a buffer amplifier and a data bus. This objection should be removed. Figure 18 indeed illustrates a buffer amplifier 240. The other occurrences of "240" in that figure do not refer to the data buses themselves but instead refer to the width of the various unnumbered data buses, as explained at col. 18, lines 17-20, that is, the number of parallel electrical lines in each of the data buses. The illustrated slanted line for the data buses is the usual convention for indicating a multi-line bus.

Figure 15 has been amended to reverse D* and R* in the lower right corner to conform to the description at page 21 lines 13 and 20.

The Examiner objects to the drawings under 37 CFR 1.83(a) as not showing every feature specified in the claims. Claims 1-4, 6, and 9 are listed below together with references to elements of the drawings upon which they read. Claim 6 has been substantially amended. It is, of course, understood that the claims may read on other circuitry.

1. A content addressable arrayed control system, comprising a plurality of control cells (254) each comprising a plurality of memory cells (312) , each memory cell receiving a respective one (D or D*) of a plurality of data lines (D_0, D_0* ... D_7, D_7*) distributed to all of said control cells and a respective one (R or R*) of a plurality of timing lines (R_0, R_0* ... R_7, R_7*) distributed to all of said control cells, and a load line (LD) distributed only to one of the control cells of said plurality of control cells, each memory cell comprising:

a 1-bit latch (332, 334, 336, 338, 340, 342)) triggered by said load line (LD) to latch a signal on said respective data line (D, D*); and

a 1-bit comparator (344, 346 or 348, 350) comparing an output of said latching circuit with a signal on said respective timing line (R or R*) and outputting a valid bit compare signal (MATCH*) on an output line commonly connected to the comparators of all memory cells of said control cell, an address compare signal on said output line being valid only when all of said comparators of said control cell output valid bit compare signals.

2. The system of Claim 1, wherein each control cell further includes an output latch (310) latching in response to said output signal a state signal (R_{8p} or R_{8p}*) on a state line distributed to all output latches of said plurality of control cells.

3. The system of Claim 2, further comprising a counter (220) driven by a clock signal (CLK) having a high-order bit (MSB) driving said state line (R_8) and

lower-order bits (8-BIT LSB) driving respective ones of said timing lines (R_7 – R_0).

4. The system of Claim 3, further comprising an address decoder (224) receiving a multi-bit address signal (A_0 – A_8) and enabling in response thereto only one of said load lines.

6. A content addressable control section (FIG 16) for controlling N time delays supplied to a plurality N of drive sections, comprising:

a multi-bit data bus (D);

N registers (362) selectively connected in parallel to said data bus;

control lines (RESET) connected to said N registers to reset said registers according to data on said data bus; and

clocked counters (364) connected to respective ones of said registers, started by trigger signals (START) and providing outputs (v_A, v_B) in comparison to said connected registers.

9. The control section of Claim 6, wherein said registers and counters are arranged in rows and columns and wherein each of registers is controlled by a row enable signal (RE), a column enable signal (CE), and a load signal (LD).

Accordingly, this drawing objection should be removed.

The Examiner has rejected claims 1-9 under 35 U.S.C. §112, ¶1 for lack of enablement. The Examiner repeats the stated deficiencies in the drawings. The discussion above for the drawing objections should fully respond to the Examiner's objections here. The Examiner further states that claims 1-4, 6, and 9 are not understood since they are not readable on the drawings. The reading of the claims above on the drawings should provide the necessary understanding. Accordingly, this rejection should be removed.

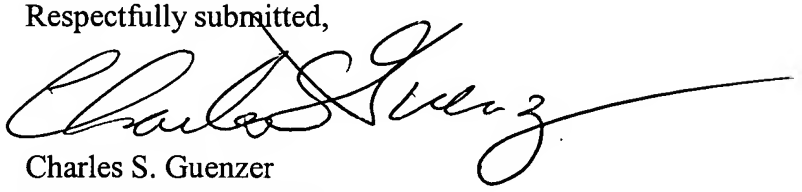
A new set of claims 10 and 11 have been added which recite many of the functions of the CAM circuitry while not requiring CAM.

Although the Examiner has cited prior art, he has issued no substantive rejection.

In view of the above amendments and remarks, reconsideration and allowance of all claims are respectfully requested. If the Examiner believes that a telephone interview would be helpful, he is invited to contact the undersigned attorney at the listed telephone number, which is on California time.

Date: 13 April 2005

Respectfully submitted,



Correspondence Address
Law Offices of Charles Guenzer
2211 Park Boulevard
P.O. Box 60729
Palo Alto, CA 94303

Charles S. Guenzer
Registration No. 30,640
(650) 566-8040

Amendments to the Drawings

Please amend FIG. 15 as indicated on the attached substitute sheet to conform to the illustrated D* and R* in the lower right corner.